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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,866	01/05/2004	Yoshitaka Mano	60188-741	3236

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EXAMINER

ENGLUND, TERRY LEE

ART UNIT	PAPER NUMBER
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2816

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/750,866

Applicant(s)

MANO ET AL.

Examiner

Terry L. Englund

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 and 9-13 is/are rejected.
- 7) ☒ Claim(s) 4-8 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 January 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 01052004.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

The "SEMICONDUCTOR DEVICE" type title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. For example, a semiconductor device is a generic type label. However, the invention itself relates to the actual relationship between the current that is selectively switched to flow through a switching transistor and an internal circuit, helping to maintain an internal voltage. Therefore, a more meaningful title, such as --Current switching for maintaining a constant internal voltage-- , is suggested.

The disclosure is objected to because of the following informality: Page 10, line 13 "pressure" should be --voltage-- for consistent labeling throughout the disclosure. Without the change, what does "pressure reduction" have to do with the present invention? An appropriate correction is required.

Claim Objections

Claims 1-13 are objected to because of the following informalities: To provide consistent labeling throughout the claims, it is suggested "switch transistor" in claims 1 (line 10), 9 (line 1), 11 (line 1), 12 (line 1), and 13 (line 8) be changed to --switching transistor--. For example, see "switching transistor" on line 5 of claim 1, and on line 4 of claim 13. It is suggested the term "the" be deleted from the phrase "is the substantially" on line 2 of claim 5 to improve word flow.

Dependent claims carry over any objection(s) from any claim(s) upon which they depend.

Appropriate corrections are required.

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3, and 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicants' own Prior Art Fig. 8, in view of Kwan. Fig. 8 shows internal voltage supply circuit 101 for generating internal voltage VINT from power supply voltage VDD, and internal circuit 103 operating from internal voltage VINT. However, the circuit shown in Prior Art Fig. 8, and its corresponding description, does not show/disclose a switching transistor and load circuit, wherein the current through the load circuit and the switching transistor is the same amount that internal circuit 103 consumes during an operation period. Fig. 1 of Kwan shows and discloses circuit with constant current $I_{sup}(t)$ flowing to internal circuit 103 and dummy load 101. Figs.

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2C and 2D show some specific examples of dummy load 101, wherein Fig. 2C's 101 and Fig. 2D's 101 directly correspond to the current consumption controls 14 and 51 shown in the applicants' own respective Figs. 1 and 4, wherein a resistor and MOS transistor are coupled in series. Kwan discloses that internal circuit 103 and dummy load 101 work together to maintain a constant current, which maintains the specified output voltage (e.g. see column 2, lines 16-19, 3643, and 52-58; column 4, lines 32-34, 53-55, and 62-65; and column 5, lines 8-13). Therefore, it would have been obvious to one of ordinary skill in the art to modify the applicants' own Prior Art Fig. 8 to incorporate the teachings of Kwan. For example, one of ordinary skill in the art would recognize memory 103 as one type of internal circuit operating from internal voltage VINT (and its related current). To help ensure voltage VINT is maintained, a dummy load type circuit (e.g. as shown and disclosed with respect to Kwan's Figs. 2C and 2D) can be added between VINT and ground, wherein the dummy load would be controlled by an output of internal circuit 103. This would be to ensure the operation of the switching transistor (within the dummy load) and internal circuit would be balanced (e.g. operate in a complementary fashion with only one being on at a time). Using Kwan's dummy load 101 shown in Fig 2C as an example, it comprises a switching transistor that would receive the operating signal output from internal circuit 103, and load circuit R that is connected to the drain of the switching transistor. With such a configuration, and the understanding of Kwan's teachings, one of ordinary skill in the art would know that when internal circuit 103 operates, it consumes current with respect to internal voltage VINT; and the switching transistor will be shut off, thus allowing the current that flows through the series connected switching transistor and load circuit R to flow into internal circuit 103. When internal circuit 103 is not operating, it requires little or no current. Therefore,

the switching transistor is turned on, allowing 103's normal operating current to flow through the switching transistor and load circuit R. For example, see Kwan's descriptions in column 5, lines 8-13, 19-21, 36-38, 54-56, and 60-63. Therefore, claim 1 is rendered obvious. By using Kwan's teachings, and dummy load type circuit, with the applicants' Prior Art Fig. 8, internal voltage VINT will be maintained whether internal circuit 103 is in operation or in a non-operation state because the total current flowing from internal voltage supply circuit 101 will be substantially constant. This will minimize inaccurate or inefficient operation due to changes within the operational status of internal circuit 103. Whether Kwan's dummy load 101 from Fig. 2C or 2D is used with the applicants' Prior Art Fig. 8, the load circuit R includes first resistor R, and it would be understood the current amount through first resistor R would be substantially the same as the current amount that would be consumed by internal circuit 103 when it is operating, thus rendering claims 2-3 obvious. Referring to Kwan's Fig. 2C dummy load 101, the switching transistor is an n-channel transistor, and its source would be grounded, and its drain would be connected to internal voltage supply circuit 101 via load circuit R, rendering claims 9-10 obvious. Referring to Kwan's Fig. 2D dummy load 101, the switching transistor is a p-channel transistor, and its source would be connected to internal voltage supply circuit 101, and its drain would be grounded via load circuit R, rendering obvious claims 11-12. [Note: Kwan's dummy load 101, as shown in Figs. 2C and 2D, was used in the descriptions above because: 1) they match the applicants' own control circuits 14 and 51, respectively; and 2) Kwan discloses the circuits shown in Figs. 2C and 2D are used with digital signal 102 (e.g. see column 5, lines 60-63), which one of ordinary skill in the art can readily equate with on/off type operations (e.g. see column 5, lines 4-13).] Interpreting the applicants' Prior Art Fig. 8, and Kwan's teachings/

dummy load 101, in a slightly different manner, it would have been obvious to one of ordinary skill in the art that the semiconductor device could be on an IC card, wherein the device includes internal voltage supply circuit 101, internal circuit 103, and Kwan's switching transistor/load circuit, as previously described. Therefore, claim 13 is also rendered obvious. Semiconductor devices are typically on some type of IC card.

No claim is allowable as presently written.

Allowable Subject Matter

However, claims 4-8 are only objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure the load circuit also includes a load adjustment section connected in series to the first resistor as recited within claim 4, upon which claims 5-8 depend.

Prior Art

The other prior art references cited on the accompanying PTO-892 are deemed relevant to at least sections of the claimed invention. Although not used in any formal rejections described above, Fig. 6 of Takahashi et al. is one example of a semiconductor device comprising internal voltage supply circuit 10 for generating internal voltage VINT from power supply voltage VDD; internal circuit 1 operated by internal voltage VINT; switching transistor 33 for receiving operation signal PA; and load circuit 43 connected to the drain of switching transistor 33, wherein switching transistor 33 is turned off when internal circuit 1 is in operation, and turned on when internal circuit 1 is in a non-operation state (e.g. see the related description of

Fig. 3 on column 10, line 46 – column 11, line 18). The reference also discloses I_o is “essentially equal to compensation current I_c plus a leakage current of internal circuit 1” when internal circuit 1 is in a non-operation state (e.g. see column 10, lines 46-57). Therefore, one of ordinary skill in the art would understand that since I_o is equal to the total current flowing through internal circuit 1 and switching transistor 33, the amount of current flowing through 33 (when it is conducting) is substantially equal to the amount of current flowing through internal circuit 1 (when it is in its normal operation state). Also shown in Fig. 6 is load 43, which can have its gate voltage varied as a means to adjust compensating current I_c (e.g. see column 12, lines 17-19). Although the Takahashi et al. reference does not clearly show or disclose switching transistor 33 receiving an operation signal from the output of internal circuit 1, it would have been obvious to one of ordinary skill in the art to apply the teachings of Kwan. This would provide a way for ensuring complementary type operation of Takahashi’s internal circuit 1 and switching transistor 33 by controlling the switching transistor with an output of the internal circuit. The reference of Luo shows/discloses circuitry that allows a current to either flow to a load or some type internal circuit, thus maintaining a current constant, and reducing charge injection (e.g. undesirable spikes – see column 1, lines 33-50). For example, in Luo’s Fig. 5, current I_A will flow either to load 440 when switch 430 is conducting, or flow to internal circuit 450 when switch MT is conducting. Since the switches operate in a complementary manner, either the load or the internal circuit must consume constant current I_A from current source 420. Therefore, these references should be carefully reviewed and considered with respect to the basic limitations claimed.

The prior art references cited on the IDS submitted Jan 5, 2004 were reviewed and considered. None of these references clearly shows or discloses a switching transistor receiving an operation signal from an internal circuit, wherein the transistor is off when the internal circuit is operating, and is on when the internal circuit is non-operating.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

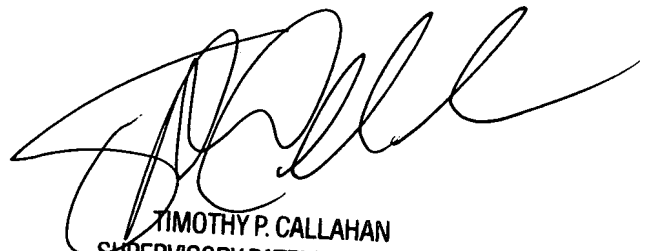
Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund

16 February 2005


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